What is Claimed:

1. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor.

2. A semiconductor device according to claim 1 wherein said semiconductor film comprises crystalline silicon.

3. A semiconductor device according to claim 1 wherein said impurity is selected from the group consisting of phosphorus and boron.

4. A semiconductor device according to claim 1 wherein said gate electrode is located over said semiconductor film.

5. A semiconductor device according to claim 1 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

6. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor and a distance between the channel forming region and the pair of first regions in ~~said first~~ thin film transistor is within a range of 0.4 to 2 μm.

7. A semiconductor device according to claim 6 wherein said semiconductor film comprises crystalline silicon.

8. A semiconductor device according to claim 6 wherein said impurity is selected from the group consisting of phosphorus and boron.

9. A semiconductor device according to claim 6 wherein said gate electrode is located over said semiconductor film.

10. A semiconductor device according to claim 6 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

11. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions

in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor and a distance between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second thin film transistor.

12. A semiconductor device according to claim 11 wherein said semiconductor film comprises crystalline silicon.

13. A semiconductor device according to claim 11 wherein said impurity is selected from the group consisting of phosphorus and boron.

14. A semiconductor device according to claim 11 wherein said gate electrode is located over said semiconductor film.

15. A semiconductor device according to claim 11 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

16. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having an inverter circuit comprising at least a second and third thin film transistors formed over the substrate for driving said active matrix circuit, at least one of said second and third thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions are overlapped with the gate electrode of said second thin film transistor.

17. A semiconductor device according to claim 16 wherein a width of the par of second regions between the channel forming region and the pair of first regions in said first thin film transistor is within a range from 0.4 to 2 μm.

18. A semiconductor device according to claim 16 wherein a width of the par of second regions between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second and third thin film transistors.

19. A semiconductor device including at least one thin film transistor, said thin film transistor comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions are overlapped with the gate electrode of said second thin film transistor.

20. A semiconductor device according to claim 19 wherein said semiconductor film comprises crystal silicon.

21. A semiconductor device according to claim 19 wherein said impurity is selected from the group consisting of phosphorous and boron.

22. A semiconductor device according to claim 19 wherein said gate electrode is located over said semiconductor film.

23. A semiconductor device according to claim 19 wherein said gate electrode comprises a multi-layered structure including first and second layers,

each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

24. A semiconductor device according to claim 19 wherein said impurity is contained in said pair of first regions in a concentration within a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3.

25. A semiconductor device according to claim 19 wherein said impurity is contained in said pair of second regions in a concentration within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.

26. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors containing:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein a sheet resistance of the pair of second regions is within a range from 10 to 50 kΩ/square.

27. A semiconductor device according to claim 26 wherein said semiconductor film comprises crystalline silicon.

28. A semiconductor device according to claim 26 wherein said impurity is selected from the group consisting of phosphorus and boron.

29. A semiconductor device according to claim 26 wherein said gate electrode is located over said semiconductor film.

30. A semiconductor device according to claim 26 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

31. A semiconductor device according to claim 26 wherein a distance between the channel forming region and the pair of first regions in said first thin film transistor is within a range of 0.4 to 5 μm.

32. A semiconductor device according to claim 26 wherein a distance between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second thin film transistor.

33. A semiconductor device according to claim 26 wherein a sheet resistance of the pair of first regions is within a range from 10 to 50 Ω/square.

34. A semiconductor device according to claim 1 wherein the concentration of said impurity in said first regions is within a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3 while the concentration of said impurity in said pair of second regions is within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.

35. A semiconductor device according to claim 6 wherein the concentration of said impurity in said first regions is with a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3 while the concentration of said impurity in said pair of second regions is within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.

36. A semiconductor device according to claim 11 wherein the concentration of said impurity in said first regions is within a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3 while the concentration of said impurity in said pair of second regions is within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.